electrically connected to said plurality of second semiconductor regions, said first main electrode further having an end extending to a boundary between the peripheral portion of said first major surface and the central portion of said first major surface;

a second main electrode formed on said second major surface of said first semiconductor layer; and

an integral semi-insulating plasma CVD nitride film for covering at least the peripheral portion of said first major surface other than the central portion of said first major surface and not extending [to] beyond an upper portion of said first gate, said integral semi-insulating plasma CVD nitride film having a conductivity which does not lose function as an insulating film and stabilizes breakdown voltage characteristics of the semiconductor device.

IN THE DRAWINGS

Approval of the attached proposed drawing changes is respectfully requested.

REMARKS

Favorable reconsideration of this application, in view of the following comments and as presently amended, is respectfully requested.

Addressing first the objection to the Reissue Declaration, a Supplemental Reissue Declaration is submitted herein that is believed to overcome the objection thereto.

Claims 1-22 are pending in this application. Claims 1-22 were rejected as based upon a defective Reissue Declaration. Claims 1-22 were rejected under 35 U.S.C. §112, second paragraph. The drawings were objected to as failing to comply with 37 C.F.R. §1.84(p)(4).

Addressing first the rejection of Claims 1-22 based upon the defective Reissue Declaration, as noted above a Supplemental Reissue Declaration is submitted herewith, which is believed to address the rejection of Claims 1-22 based on the defective Reissue Declaration.

Addressing now the rejection of Claims 1-22 under 35 U.S.C. §112, second paragraph, that rejection is traversed by the present response.

Claims 1 and 12 are amended by the present response as suggested in the Office Action to clarify the noted language. Claims 1-22 are now believed to be in full compliance with all requirements under 35 U.S.C. §112, second paragraph.

Addressing now the objections to the drawings, those rejections are traversed by the present response.

It is first noted that proposed drawing changes are submitted with the present response to delete the improper reference character 16 in Figure 8. That proposed drawing change is believed to also address the objection noted at column 11, line 26.

The specification has also been amended at column 11, line 36, and at column 1, line 48, to be consistent with the drawings to overcome the objection to those portions in the specification.

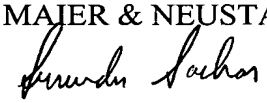
It should also be noted that the amendment at column 11, line 36, addresses an error which appears to have been introduced by the U.S. PTO in that the original specification correctly recited the "passivation film 12". An error in printing on the part of the U.S. PTO appears to have caused the error being corrected at column 11, line 36.

In view of the presently submitted proposed drawing changes and amendments to the specification, the outstanding objections to the drawings are believed to be overcome by the present response.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Gregory J. Maier
Attorney of Record
Registration No. 25,599
Surinder Sachar
Registration No. 34,423

22850

(703) 413-3000
Fax No.: (703)413-2220
SNS/rac
I:\atty\SNS\198786US-AM.wpd

Marked-Up Copy
Serial No:
09/891,925
Amendment Filed on:
5-30-02

IN THE SPECIFICATION

Please replace the paragraph at column 1, lines 40-60, as follows:

--Referring to FIG. 21, the semiconductor body 4 is initially formed, and the P^+ base layer 5, and P wells, P^+ layers serving as the guard rings 11 are formed in the surface of the N^- layer 3 of the semiconductor body 4. The gate insulating film 7 of silicon oxide is formed on the surface of the P^+ base layer 5, and a polysilicon film is formed on the surface of the gate insulating film 7. Then the N^+ emitter layer 6 and the channel stopper 15 are formed by diffusion, and the passivation films 12 and [17] 18 are formed. The gate interconnection line 9 and the emitter electrode 10 are formed as Al electrodes. Thereafter, the surface protective film 14 is formed to cover the IGBT surface except the emitter wire bonding region 13 and the gate bonding pad which is a part of the gate interconnection line 9. A silicon nitride film serving as the surface protective film 14 is formed by plasma CVD process (referred to hereinafter as P-CVD process) at a temperature of about 300 to 400° C. in an atmosphere of a mixed silane-ammonia gas. Then the IGBT is exposed to radiation for lifetime control thereof and is subjected to heat treatment at a temperature of 300 to 400° C. to eliminate distortion resulting from the radiation.--

Please replace the paragraph beginning at column 2, line 52, to column 3, line 9 as follows:

--The silicon nitride film formed by the P-CVD process contains a large amount of hydrogen atoms. For example, the number of Si-H chemical bonds in the silicon nitride film formed by the P-CVD process is $1.0x10^{22}$ cm^{-3} to $1.6x10^{22}$ cm^{-3} by measurement using FT-IR (Fourier transform infrared spectroscopy) technique. The number of Si-H chemical bonds in the PSG film is on the order of $0.4x10^{22}$ cm^{-3}. The hydrogen atoms in the silicon nitride film readily migrate through the surface protective film 14 of silicon nitride, the aluminum electrodes such as the gate interconnection line 9 and emitter electrode 10, the passivation film [17] 12 and the gate insulating film 7 of silicon oxide depending upon the atmospheric temperatures and the polarity and magnitude of the applied voltage to reach a silicon-silicon oxide interface at the surface of the semiconductor body 4 without difficulty. Dangling bonds at the silicon-silicon oxide interface are bonded to hydrogen atoms from the silicon nitride film to form Si-H chemical bonds at the silicon-silicon oxide interface, resulting in an unstable interface state. It takes time to stabilize the interface state, which is considered to cause the difficulty in saturating the varying threshold voltage V_{th}.--

Please replace the paragraph at column 11, lines 36-38, as follows:

--The passivation films [15] 12 and 18 of PSG are formed on the top surface, and electrode contact portions are etched (FIG. 10).--

IN THE CLAIMS

--1. (Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type having first and second major surfaces;

a first semiconductor region of a second conductivity type formed selectively in said first major surface of said first semiconductor layer so that said first semiconductor layer is exposed in a peripheral portion of said first major surface and said first semiconductor layer is exposed in the form of an insular region in a central portion of said first major surface;

a second semiconductor region of the first conductivity type formed in a surface of said first semiconductor region, with a channel region provided between said second semiconductor region and said insular region of said first semiconductor layer;

a gate insulating film formed on a surface of said channel region;

a first gate formed on said gate insulating film;

an interlayer insulating film formed at least on said first gate:

a first main electrode formed over a surface of said interlayer insulating film and covering a surface of said second semiconductor region, said first main electrode being electrically connected to said second semiconductor region and having an end extending to a boundary between the peripheral portion of said first major surface and the central portion of said first major surface;

a second main electrode formed on said second major surface of said first semiconductor layer; and

an integral semi-insulating plasma CVD nitride film covering at least the peripheral portion of said first major surface other than the central portion of said first major surface and not extending [to] beyond an upper portion of said first gate, said integral semi-insulating plasma CVD nitride film having a conductivity which does not lose function as an insulating film and stabilizes breakdown voltage characteristics of the semiconductor device.

12. (Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type having first and second major surfaces;

at least one first semiconductor region of a second conductivity type formed selectively in said first major surface of said first semiconductor layer so that said first semiconductor layer is exposed in a peripheral portion of said first major surface and said first semiconductor layer is exposed in the form of a plurality of insular regions in a central portion of said first major surface;

a plurality of second semiconductor regions of the first conductivity type formed in a surface of said at least one first semiconductor region, with channel regions provided between said second semiconductor regions and said insular regions of said first semiconductor layer;

a gate insulating film formed on a surface of said channel regions;

a first gate formed on said gate insulating film;

an interlayer insulating film formed at least on said first gate[:];

a first main electrode formed over a surface of said interlayer insulating film and covering a surface of said second semiconductor region, said first main electrode being electrically connected to said plurality of second semiconductor regions, said first main electrode further having an end extending to a boundary between the peripheral portion of said first major surface and the central portion of said first major surface;

a second main electrode formed on said second major surface of said first semiconductor layer; and

an integral semi-insulating plasma CVD nitride film for covering at least the peripheral portion of said first major surface other than the central portion of said first major surface and not extending [to] beyond an upper portion of said first gate, said integral

semi-insulating plasma CVD nitride film having a conductivity which does not lose function as an insulating film and stabilizes breakdown voltage characteristics of the semiconductor device.--